Remarks

Claims 1-30 are pending in the application. Claims 1, 2, 4-9, 11-16, 18, 19, 21, 22 and 24-30 have been rejected under 35 U.S.C. § 102(b). In view of the following remarks, reconsideration and withdrawal of these grounds of rejection is requested.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 2, 4-9, 11-14, 21, 22, 24-28 and 30 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Dening et al. (U.S. Pat. No. 6,313,705). Independent claims 8 and 21 have been cancelled in favor of new independent claims 10 and 23, and thus only claims 1, 2, 4-7, 27, 28 and 30 are at issue here. For the reasons set forth below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

The present invention comprises, in one exemplary embodiment, a power amplification control circuit 100 including a first transistor 108, a second transistor 118, a ballast resistor 116 and a feedback stabilization circuit 106. The feedback stabilization circuit comprises, in one exemplary embodiment, a resistor 105 and a capacitor 107.

Independent claim 1 recites:

> A circuit comprising: a first transistor; a second transistor; a ballast resistor coupled between an emitter terminal of the first transistor and a base terminal of the second transistor; and, a feedback stabilization circuit coupled to the first transistor, wherein a control voltage applied to a base terminal of the first transistor controls the amplification of a signal applied to the base terminal of the second transistor. [emphasis added].

Thus, claim 1 requires at least a "feedback stabilization circuit." Dening fails to disclose, teach or suggest such a circuit.

Dening teaches a bias network 1000 which includes a first transistor Q2 with its base coupled to a voltage bias V_{bias}, and a second transistor Q1 with a resistor R6 coupled to its base (See Fig. 10). The bias network 1000 also includes a resistor R3 coupled between the emitter of the transistor Q2 and the voltage bias V_{bias}.

Dening fails to disclose, teach or suggest a "feedback stabilization circuit." The Examiner asserts, on page 2 of the Office Action, that the resistor R3 shown in Figure 10 of Dening comprises a "feedback stabilization circuit"; the Applicant strenuously disagrees. Dening explicitly states that the purpose of R3 is to adjust the "impedance of the bias network [1000]" (see, col. 6, lines 28-30)[1]. As is well known and understood in the art, impedance adjustment and matching are wholly different functions from "feedback stabilization." Moreover, it would be an error for the Examiner to arbitrarily assign a function (e.g., "feedback stabilization") to an element (e.g., R3) which is different from the function explicitly taught by the specification. Accordingly, because Dening fails to disclose or suggest any element or circuit which performs "feedback stabilization," reconsideration and withdrawal of this ground of rejection with respect to independent claim 1, and claims 2 and 4-7 dependent thereon, is respectfully requested.

With respect to independent claim 27, this claim includes a similar limitation to the one discussed above with reference to claim 1. In particular, claim 27 includes the limitation of

1 The description appearing at col. 6, lines 28-30 of the Dening patent references Figure 9. However, Dening later states that "the bias network 1000 is similar to the bias network 900 illustrated in FIG. 9, except that the bias voltage source Vbias 1002 is combined with a pair of diode connected transistors 1004..." (see, col. 6, lines 39-43).

"providing feedback stabilization of [a] control signal." As argued above, Dening nowhere discloses, teaches or suggests a circuit for providing feedback stabilization of a control (or other) signal. The results of feedback stabilization can be seen in Figures 7(a) and 7(b) of the present application. Hence, reconsideration and withdrawal of this ground of rejection is respectfully requested.

With respect to independent claim 28, Dening fails to disclose, teach or suggest a method for amplifying a signal which includes the step of "providing a circuit to compensate for temperature variations" (emphasis added). Dening nowhere discusses temperature variations, or any means of compensating for such variations. Moreover, the Examiner has failed to address the limitation of "providing a circuit to compensate for temperature variations" anywhere in the Office Action. Therefore, reconsideration and withdrawal of this ground of rejection is respectfully requested.

With respect to independent claim 30, Dening fails to disclose, teach or suggest a method for amplifying a signal which includes the step of "providing at least one resistor coupled between the base terminal and the emitter terminal of the first transistor to reduce the power control waveform slope" (emphasis added). Dening nowhere discusses reducing a power control waveform slope. Additionally, the Examiner has failed to address the limitation of "providing at least one resistor coupled between the base terminal and the emitter terminal of the first transistor to reduce the power control waveform slope" anywhere in the Office Action. Accordingly, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Accordingly, the statements in this section regarding resistor R3 are relevant to bias circuit 1000 (Fig. 10).

Claims 15, 16, 18, 19 and 29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Järvinen (U.S. Pat. No. 6,052,032). Independent claim 15 has been canceled in favor of new independent claim 17, which was previously indicated as containing allowable subject matter. Accordingly, the rejection of claim 15, 16, 18 and 19 is deemed moot.

With reference to independent claim 29, Järvinen fails to disclose, teach or suggest a method for amplifying a signal which includes the step of "providing at least one bypass capacitor coupled to a collector terminal of the first transistor to improve peak operating performance" (emphasis added). Järvinen nowhere discusses peak operating performance, or any means of improving such performance. Moreover, the Examiner has failed to address the limitation of "providing at least one bypass capacitor coupled to a collector terminal of the first transistor to improve peak operating performance" anywhere in the Office Action. The results obtained when a bypass capacitor is included can be seen in Figures 5(a), 5(b), 6(a), 6(b), 7(a) and 7(b) of the present application. Thus, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

Respectfully submitted,

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